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(54) **METHOD OF STRESSING A SEMICONDUCTOR LAYER**

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H01L 29/78	(2006.01)
H01L 27/12	(2006.01)
H01L 21/02	(2006.01)

(52) **U.S. Cl.**

CPC ***H01L 21/76283*** (2013.01); ***H01L 21/02356*** (2013.01); ***H01L 21/02532*** (2013.01); ***H01L 21/76237*** (2013.01); ***H01L 27/1203*** (2013.01); ***H01L 29/7846*** (2013.01); ***H01L 29/7847*** (2013.01); ***H01L 29/7849*** (2013.01)

(58) **Field of Classification Search**

CPC H01L 21/02356; H01L 21/02532; H01L 21/76237; H01L 21/76283; H01L 27/1203; H01L 29/7846; H01L 29/7847; H01L 29/7849

USPC 438/149, 156–158, 283–284, 403–404, 438/424–425, 427–428, 436–437

See application file for complete search history.

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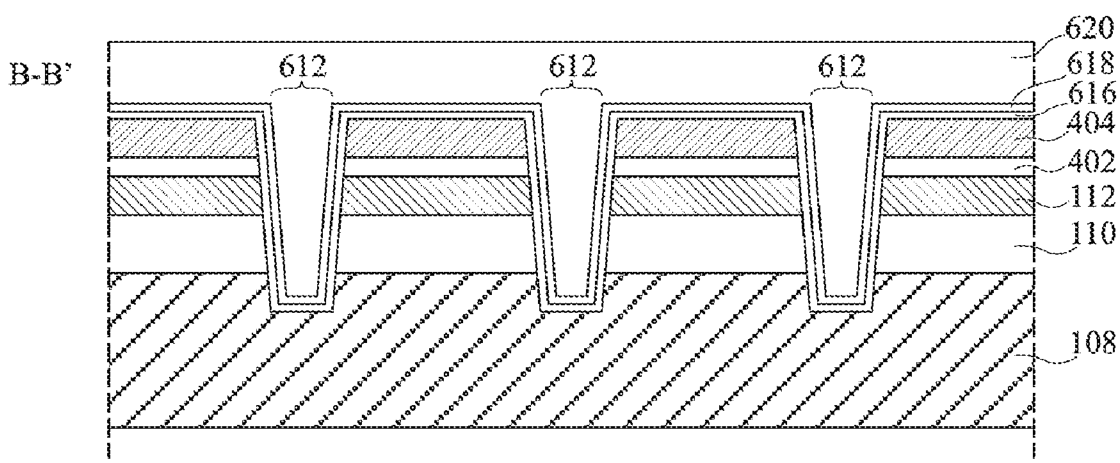
Primary Examiner — H Tsai

(74) *Attorney, Agent, or Firm* — Seed IP Law Group PLLC

(57) **ABSTRACT**

One or more embodiments of the disclosure concerns a method of forming a stressed semiconductor layer involving: forming, in a surface of a semiconductor structure having a semiconductor layer in contact with an insulator layer, at least two first trenches in a first direction; introducing, via the at least two first trenches, a stress in the semiconductor layer and temporally decreasing, by annealing, the viscosity of the insulator layer; and extending the depth of the at least two first trenches to form first isolation trenches in the first direction delimiting a first dimension of at least one transistor to be formed in the semiconductor structure.

26 Claims, 10 Drawing Sheets



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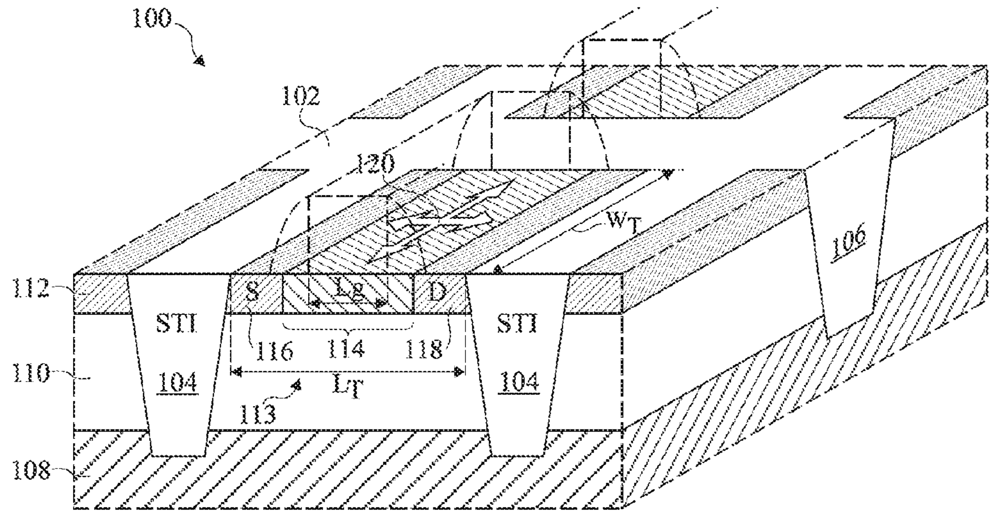

100
102
120
W_T
106
112
STI
S
L_g
D
STI
116
114
118
110
104
L_T
104
113
108

Fig 1A

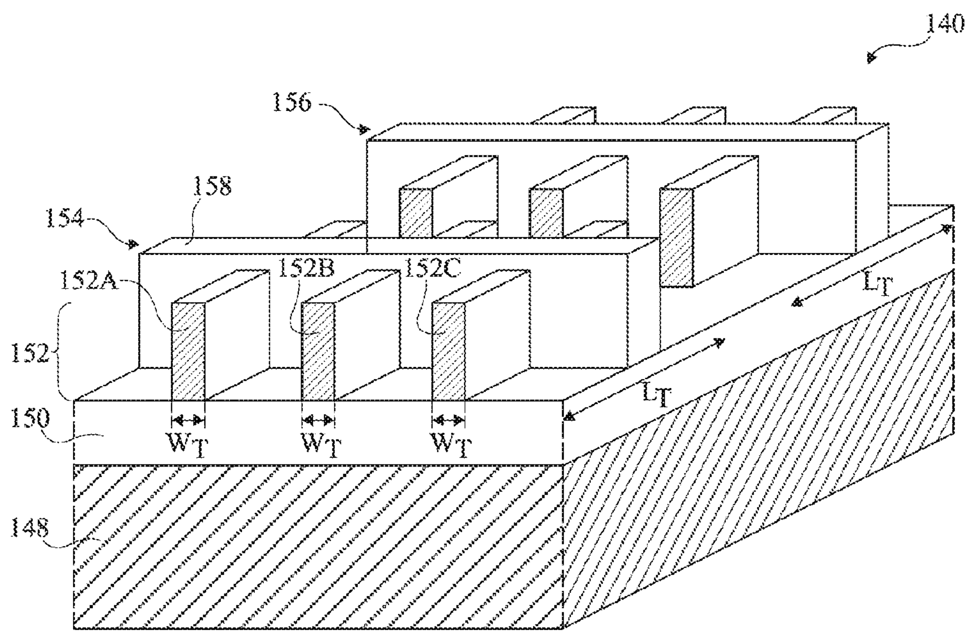

140
156
158
154
152A
152B
152C
152
150
W_T
W_T
W_T
L_T
L_T
148

Fig 1B

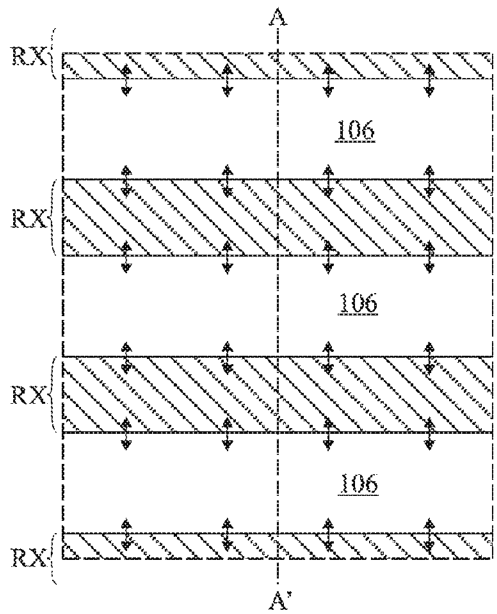


Fig 2A

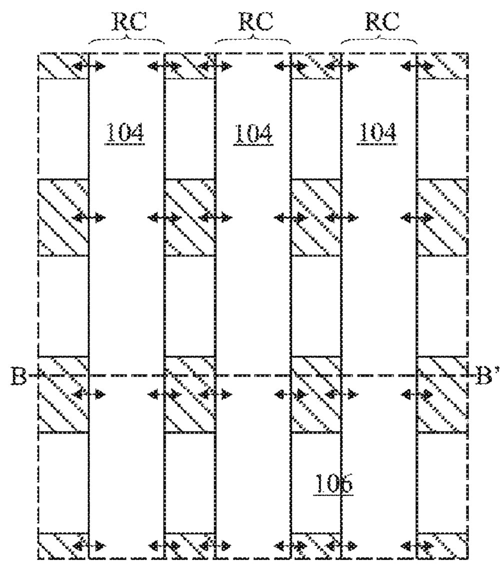


Fig 2B

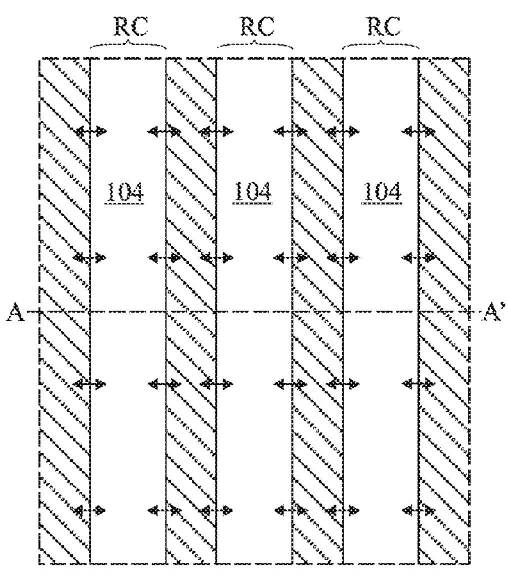


Fig 3A

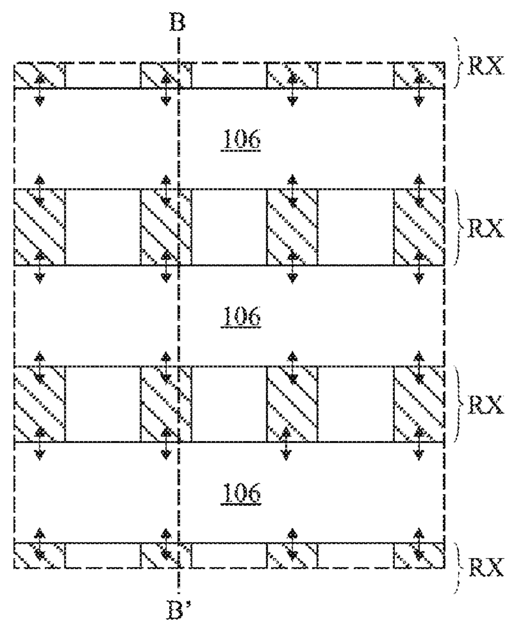
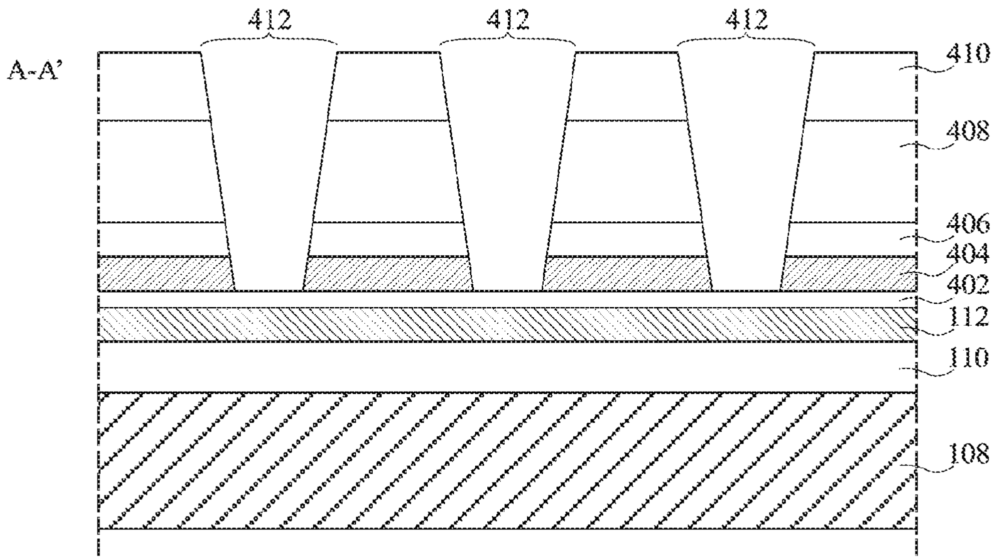


Fig 3B



412
412
412
A-A'
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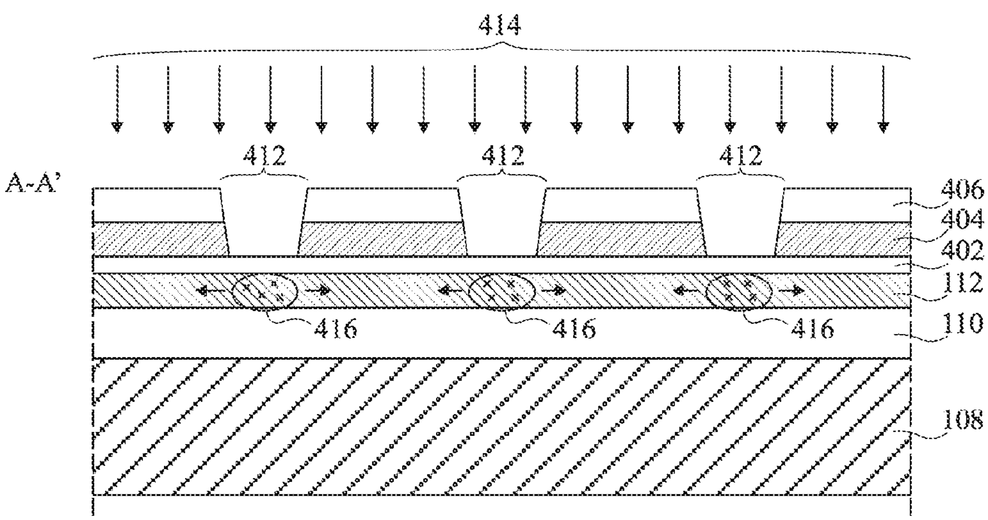
112
110
108

Fig 4A



414
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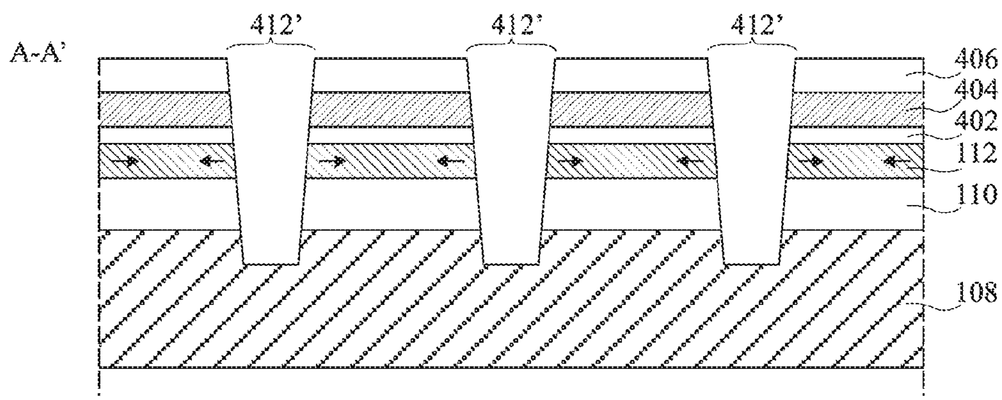
108

Fig 4B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412'
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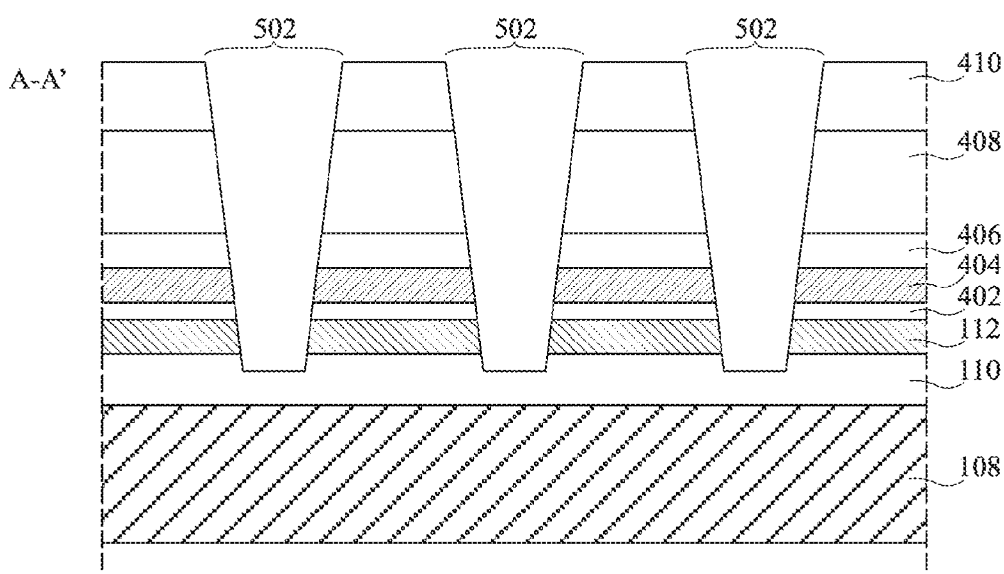
402
112
110
108

Fig 4C


A-A'
502
502
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410
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112
110
108

Fig 5A

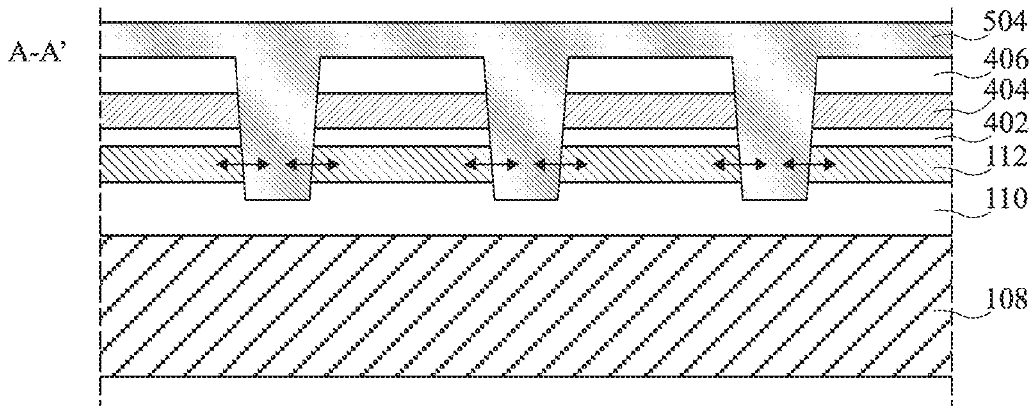

Fig 5B

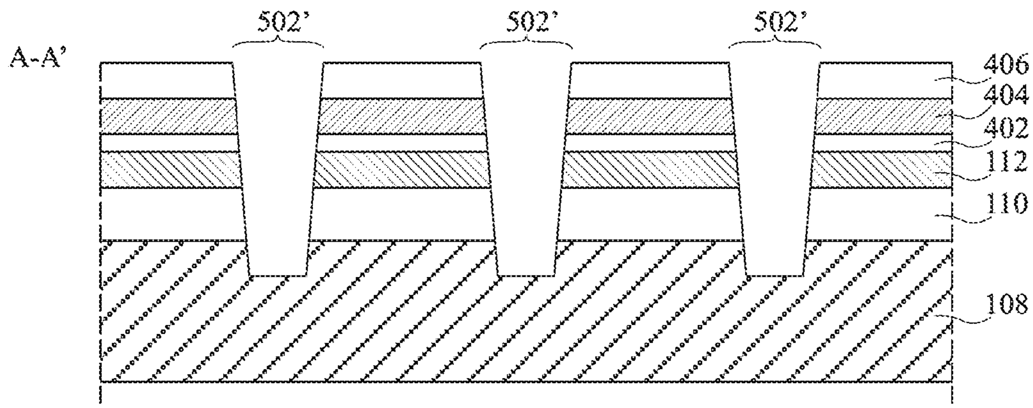

Fig 5C

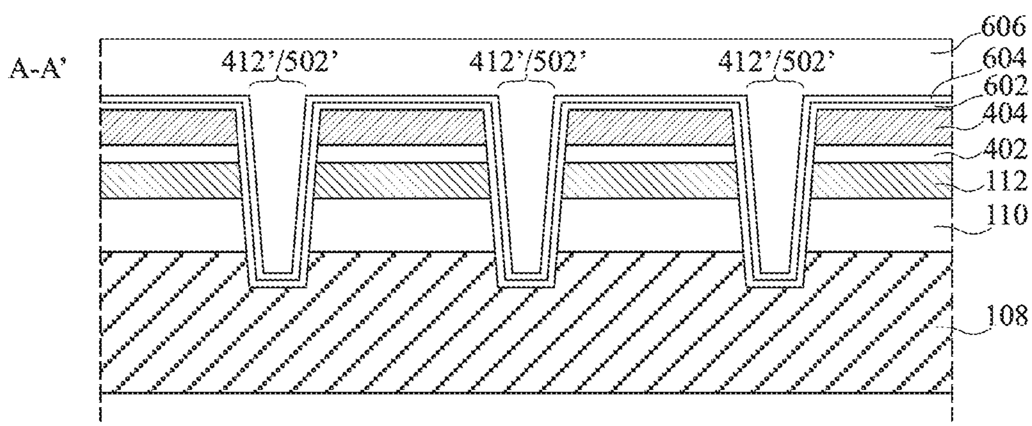

Fig 6A

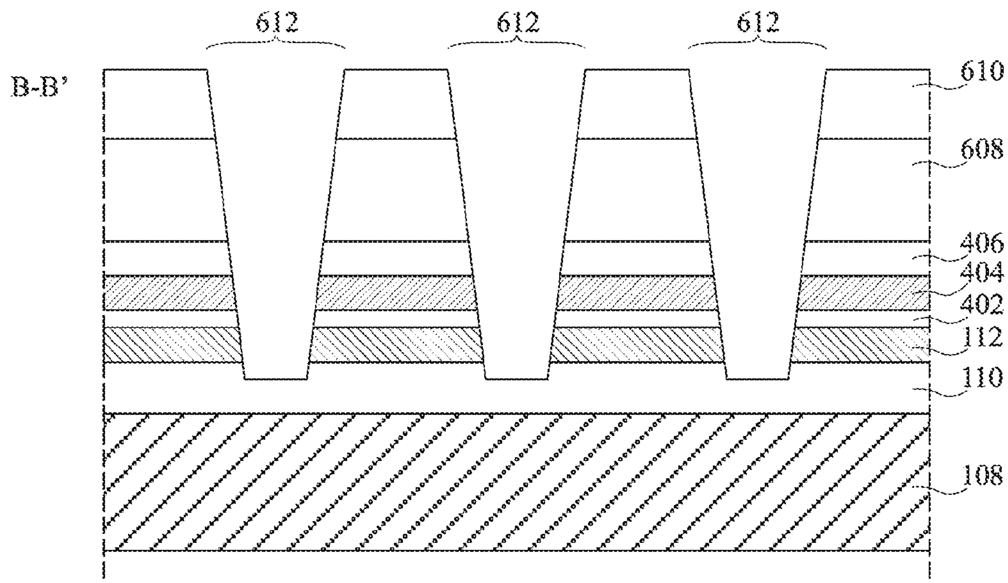

Fig 6B

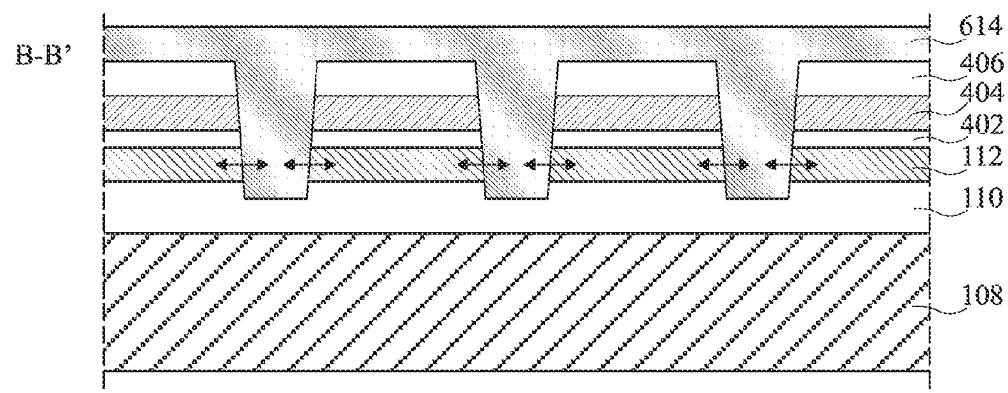

Fig 6C

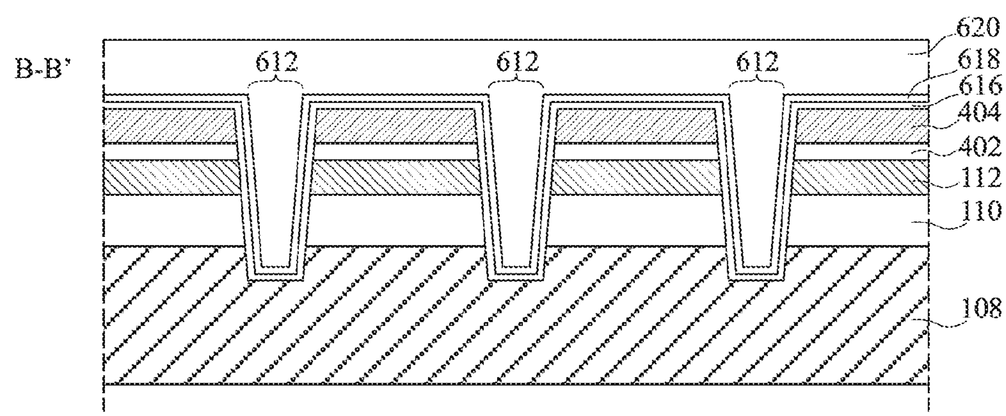

Fig 6D

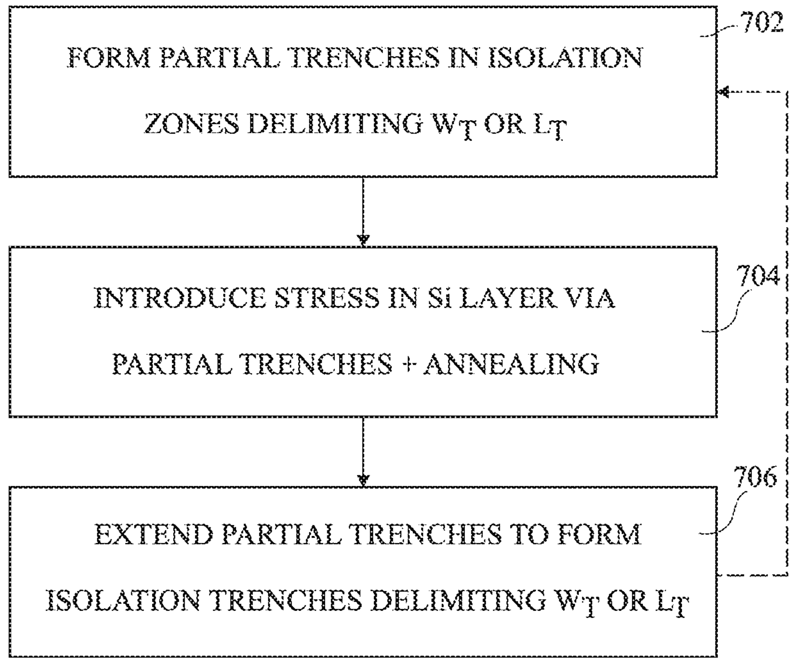

Fig 7

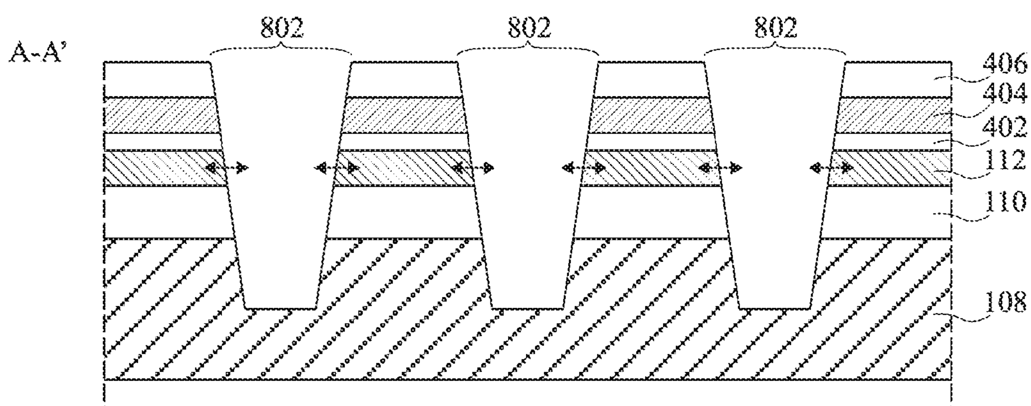

Fig 8A

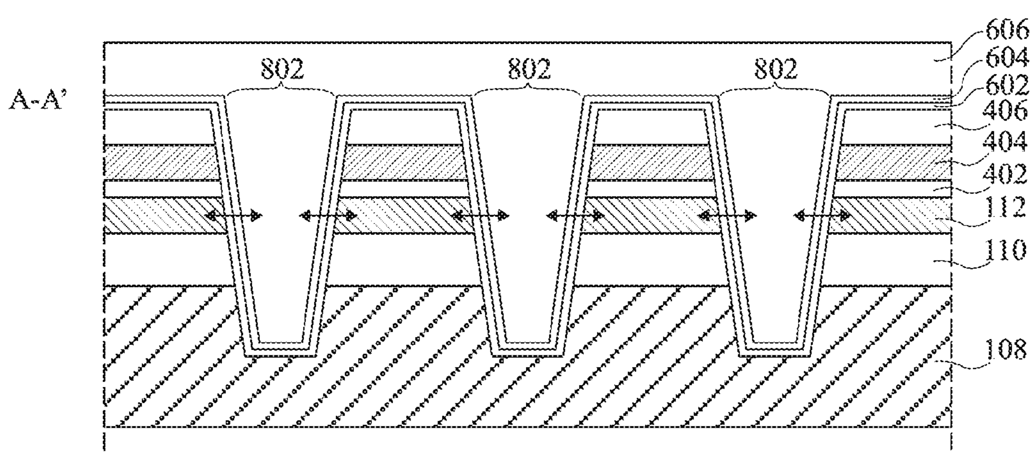

Fig 8B

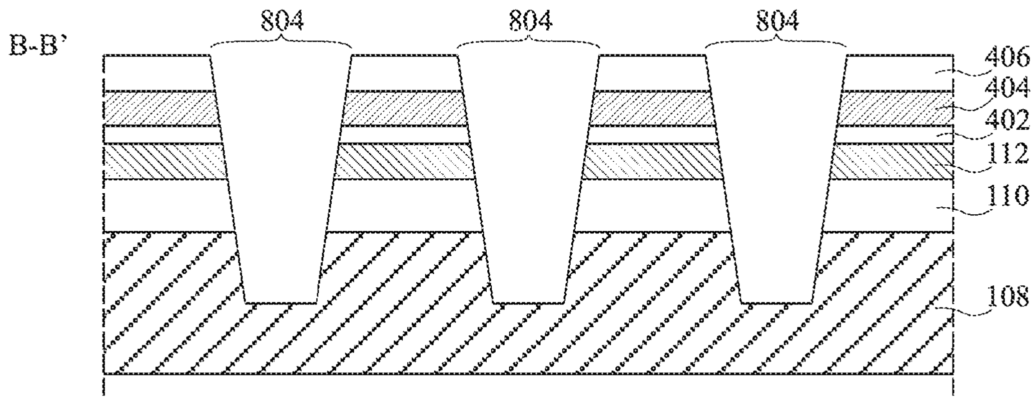

Fig 8C

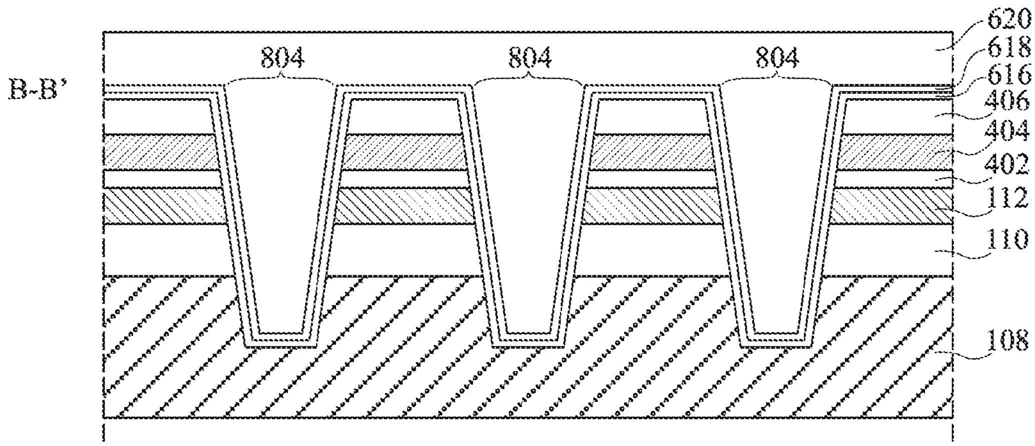

Fig 8D

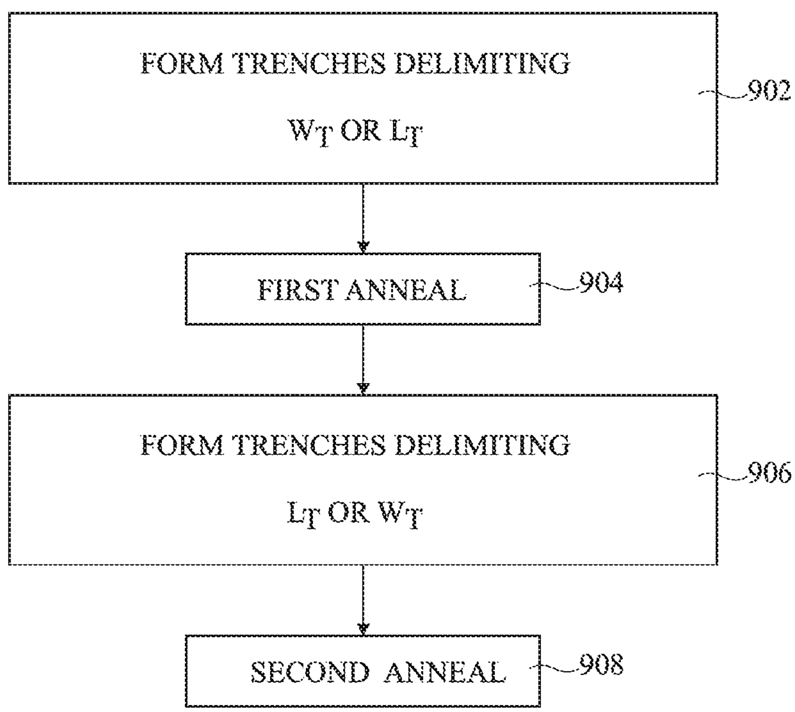

Fig 9

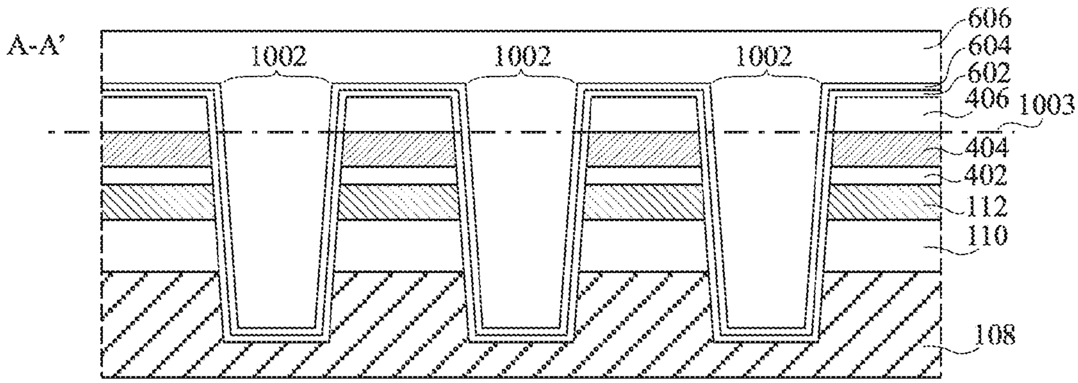

Fig 10A

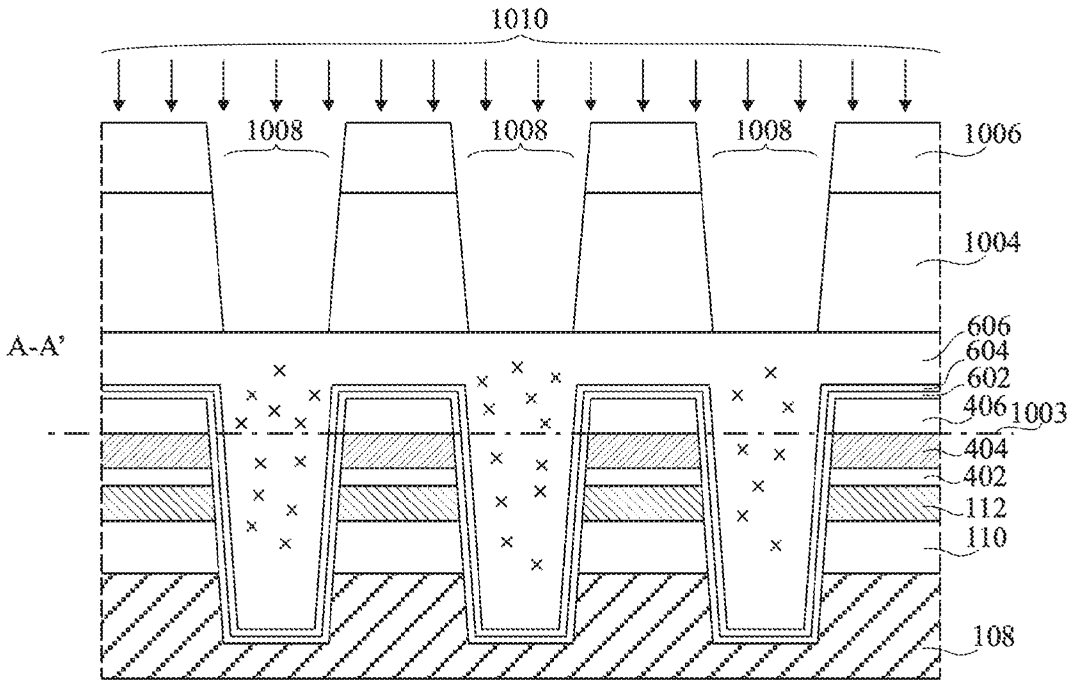

Fig 10B

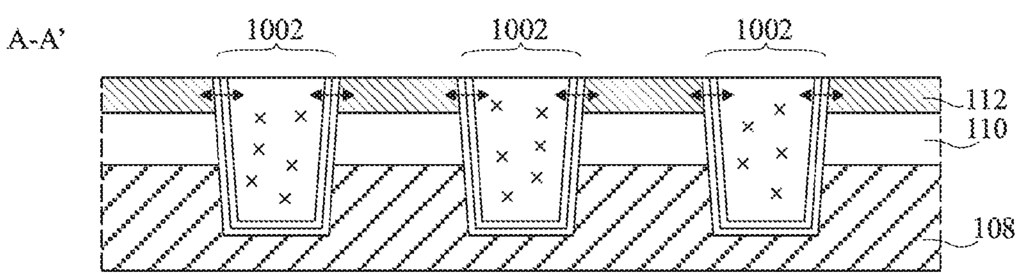

Fig 10C

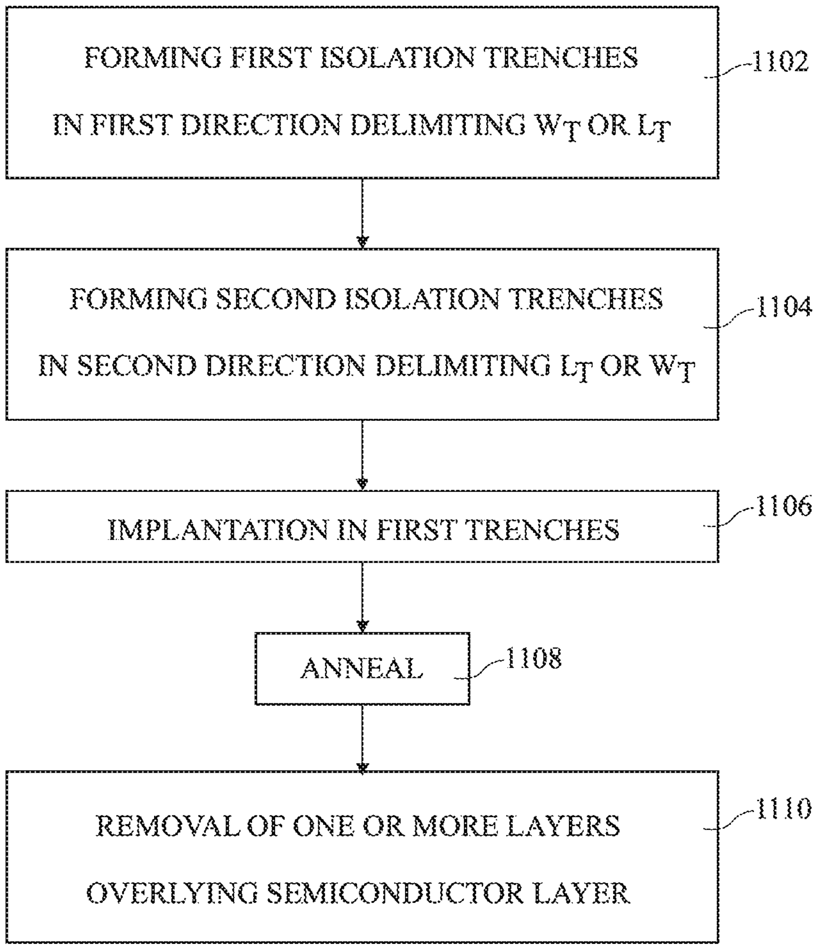
FORMING FIRST ISOLATION TRENCHES IN FIRST DIRECTION DELIMITING W_T OR L_T
1102
FORMING SECOND ISOLATION TRENCHES IN SECOND DIRECTION DELIMITING L_T OR W_T
1104
IMPLANTATION IN FIRST TRENCHES
1106
ANNEAL
1108
REMOVAL OF ONE OR MORE LAYERS OVERLYING SEMICONDUCTOR LAYER
1110

Fig 11

METHOD OF STRESSING A SEMICONDUCTOR LAYER

BACKGROUND

1. Technical Field

The present disclosure relates to the field of stressed semiconductor layers, and in particular to a method for forming a stressed semiconductor layer.

2. Description of the Related Art

The performance of certain types of transistors such as p-channel and re-channel MOS transistors can be greatly improved by the introduction of stress into the channel region.

In particular, for PMOS transistors, the presence of compressive stress in the channel region generally leads to an increase in hole mobility, and thus an improvement in terms of switching speed.

For NMOS transistors, the presence of tensile stress in the channel region generally leads to an increase in the electron mobility, and thus an improvement in terms of switching speed.

However, existing transistor processing methods generally lead to transistors having channels that are stressed in a non-optimal fashion, leading to non-optimal transistor performance. There is thus a need for a method of forming a stressed semiconductor layer leading to increased transistor performance.

BRIEF SUMMARY

One or more embodiments are directed to stressed semiconductor layers, and methods for forming a stressed semiconductor layer.

According to one embodiment, there is provided a method of forming a stressed semiconductor layer comprising: forming, in a surface of a semiconductor structure having a semiconductor layer in contact with an insulator layer, at least two first trenches in a first direction; introducing, via the at least two first trenches, a stress in the semiconductor layer and temporally decreasing, by annealing, the viscosity of the insulator layer; and extending the depth of the at least two first trenches to form first isolation trenches in the first direction delimiting a first dimension of at least one transistor to be formed in the semiconductor structure.

According to one embodiment, introducing a stress in the semiconductor layer comprises the introduction of a first material via the at least two first trenches and annealing, and extending the at least two first trenches comprises at least partially removing the first material.

According to one embodiment, the introduction of the first material comprises: implanting atoms of the first material into a region of the semiconductor layer underlying each of the at least two first trenches; or depositing the first material to at least partially fill each of the at least two first trenches, and heating the first material during the annealing step.

According to one embodiment, the introduction of the first material comprises implanting atoms of the first material into regions of the semiconductor layer, the at least two first trenches not extending deeper than the surface of the semiconductor layer.

According to one embodiment, the first material is germanium.

According to one embodiment, the introduction of the first material comprises depositing the first material to at least partially fill each of the two first trenches, and the at least two first trenches extend through the semiconductor layer and at least partially into the insulator layer.

According to one embodiment, the introduction of the first material comprises depositing a metal to at least partially fill the at least two first trenches.

According to one embodiment, the first material has a coefficient of thermal expansion different to than that of the material of the semiconductor layer.

According to one embodiment, the first material has a first coefficient of thermal expansion different to that of the material of the semiconductor layer, the method further comprising, prior to temporally decreasing the viscosity of the insulator layer: forming, in the surface of the semiconductor structure, at least two second trenches in a second direction; depositing a second material to at least partially fill each of the at least two second trenches, wherein the second material has a second coefficient of thermal expansion different to that of the first material and that of the material of the semiconductor layer; and extending the depth of the at least two second trenches to form second isolation trenches in the second direction delimiting a second dimension of the at least one transistor to be formed in the SOI structure.

According to one embodiment, the method further comprises forming at least two second isolation trenches in a second direction delimiting a second dimension of the at least one transistor.

According to one embodiment, forming the at least two second isolation trenches is performed after the step of temporally decreasing the viscosity of the insulator layer.

According to one embodiment, temporally decreasing the viscosity of the insulator layer comprises annealing at between 950° C. and 1150° C. for at least 20 minutes.

According to one embodiment, the semiconductor structure is an SOI (semiconductor on insulator) structure.

According to one embodiment, the semiconductor layer comprises a plurality of semiconductor fins.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

The foregoing and other features and advantages will become apparent from the following detailed description of embodiments, given by way of illustration and not limitation with reference to the accompanying drawings, in which:

FIG. **1**A is a perspective view of a portion of a semiconductor on insulator (SOI) structure comprising transistors according to an example embodiment of the present disclosure;

FIG. **1**B is a perspective view of a portion of a semiconductor structure comprising transistors according to a further example embodiment of the present disclosure;

FIGS. **2**A and **2**B are plan views of masks used for forming trenches in the semiconductor structure of FIG. **1**A or lB during a method of forming a stressed semiconductor layer according to an example embodiment of the present disclosure;

FIGS. **3**A and **3**B are plan views of masks used for forming trenches in the semiconductor structure of FIG. **1**A or lB during a method of forming a stressed semiconductor layer according to a further example embodiment of the present disclosure;

FIGS. **4**A to **4**C are cross-section views of an SOI structure at various stages during a method of forming a stressed semiconductor layer according to an example embodiment of the present disclosure;

FIGS. **5**A to **5**C are cross-section views of the SOI structure at various stages during a method of forming a stressed semiconductor layer according to a further example embodiment of the present disclosure;

FIGS. **6**A to **6**D are cross-section views of the SOI structure at various stages during a method of forming a stressed semiconductor layer according to an example embodiment of the present disclosure;

FIG. **7** is a flow diagram illustrating steps in a method of forming a stressed semiconductor layer according to an example embodiment of the present disclosure;

FIGS. **8**A and **8**B are cross-section views of the SOI structure at various stages during a method of forming a semiconductor layer with uniaxial stress according to an example embodiment of the present disclosure;

FIGS. **8**C and **8**D are cross-section views of the SOI structure at various stages during a method of forming a semiconductor layer with uniaxial stress according to an example embodiment of the present disclosure;

FIG. **9** is a flow diagram illustrating steps in a method of forming a semiconductor layer with uniaxial stress according to an example embodiment of the present disclosure;

FIGS. **10**A to **10**C are cross-section views of the SOI structure at various stages during a method of forming a semiconductor layer with uniaxial stress according to an example embodiment of the present disclosure; and

FIG. **11** is a flow diagram illustrating steps in a method of forming a semiconductor layer with uniaxial stress according to an example embodiment of the present disclosure.

DETAILED DESCRIPTION

FIG. **1**A is a perspective view of a portion **100** of a semiconductor on insulator (SOI) structure. The SOI structure comprises a grid **102** of isolation trenches, which are for example shallow trench isolations (STI), delimiting transistors. In particular, vertical trenches **104**, of which two are illustrated in the portion **100** of FIG. **1**A, delimit one dimension of each transistor, while horizontal trenches **106**, of which one is illustrated in FIG. **1**A, delimit another dimension of each transistor. Throughout the present description, the term "vertical" is used to designate a direction of the trenches depicted as generally running from top to bottom on the page, while the term "horizontal" is used to designate a direction of the trenches depicted as generally running from left to right on the page.

In the example of FIG. **1**A, the SOI structure comprises a substrate **108**, for example formed of bulk silicon, a layer of insulator **110** formed over the substrate **108**, and a semiconductor layer **112**, formed over and in contact with the insulator layer **110**. The insulator layer **110** is for example between 20 and 50 nm in thickness, and corresponds to a buried oxide layer. The semiconductor layer **112** is for example between 5 and 20 nm in thickness. The semiconductor layer **112** is for example formed of silicon or SiGe.

The isolation trenches **104**, **106** for example extend through the semiconductor layers **112** and at least partially into the insulator layer **110**. In the example of FIG. **1**A, the trenches **104**, **106** also extend into the substrate **108**. The isolation trenches **104**, **106** for example have a depth of between 7 and 300 nm.

FIG. **1**A illustrates an example of a portion of a transistor **113** formed in the semiconductor layer **112**, and delimited by the isolation trenches **104** and **106**. The transistor **113** is for example a p-channel or n-channel MOS transistor. In the example of FIG. **1**A, the transistor **113** comprises, between the two trenches **104**, a central channel region **114**, and source and drain regions **116**, **118** on respective sides of the channel region **114**. The source and drain regions **116**, **118** are for example heavily doped regions of the semiconductor layer **112**.

As represented by dashed lines in FIG. **1**A over the channel region **114** of transistor **113**, a gate stack will for example be formed having spacers partially overhanging the source and drain regions **116**, **118**. The gate length L_g of the transistor is defined as the length of the gate in the direction perpendicular to direction that the isolation trenches **104** are formed. In the same direction as the gate length L_g, a transistor length L_T is defined herein as the length of the transistor from the outer edge of the source region **116** to the outer edge of the drain region **118**. This transistor length L_T corresponds to the distance between the inner edges of the isolation trenches **104** that delimit the transistor, and is for example in the range of 50 to 150 nm.

In the perpendicular direction to the gate length L_g, and in the same direction as the one in which the isolation trenches **104** are formed, a transistor width W_T is defined herein as the width of the semiconductor layer **112** between the pair of isolation trenches **106** that delimit the transistor, and is for example in the range of 50 to 100 nm. In the example of FIG. **1**A, for ease of illustration, only one of the isolation trenches **106** delimiting the transistor width W_T of transistor **113** is illustrated.

The isolation trenches **104** and **106** for example have inclined sides, and the transistor lengths L_T and widths W_T are for example measured from the widest section of the trenches, which is for example at the surface of the semiconductor layer **112**.

While not illustrated in FIG. **1**A, there may be hundreds or thousands of p-channel or n-channel transistors formed in the SOI structure and delimited by the grid **102** of isolation trenches **104**, **106**. Each of these transistors is for example orientated in the same direction, for example having a transistor length L_T in the horizontal direction, and a transistor width W_T in the vertical direction.

As shown by biaxial arrows **120** positioned over the channel region **114** of the semiconductor layer **112** in FIG. **1**A, the semiconductor layer **112** is for example stressed. This stress can be a compressive stress, or a tensile stress, and may be biaxial, in other words in both the directions of the transistor length L_T and width W_T, or uniaxial, in other words in either the direction of the transistor length L_T, or in the direction of the transistor width W_T. However, the term "uniaxial stress" will also be used to cover the case in which there is biaxial stress, but the stress levels are different along the transistor's length and width, the stress along one of these directions being for example relatively low or negligible.

FIG. **1**B is a perspective view of a portion **140** of a semiconductor structure according to an alternative embodiment based on finFET transistors.

The semiconductor structure **140** comprises a substrate **148**, for example formed of bulk silicon, and a layer of insulator **150** formed over the substrate **148**. A semiconductor layer **152** is formed over and in contact with the insulator layer **150**, and comprises semiconductor fins defining two transistor devices **154**, **156** positioned side by side. The device **154** comprises fins **152**A, **152**B, **152**C, each corresponding to a separate transistor, having a p-type or n-type channel, and controlled by a common gate **158** formed substantially perpendicular to the fins **152**A to **152**C, and covering a mid-portion of each of the fins. The insulator layer **150** is for example between 20 and 50 nm in thickness and corresponds to a buried oxide layer. The semiconductor layer **152**, and in particular each of the fins **152**A to **152**C, is for example between 20 and 50 nm in thickness. The fins are for example formed of silicon or SiGe. The device **156** is for example identical to device **154**.

The width W_T of each transistor in the structure of FIG. 1B corresponds to the width of each fin, while the length L_T of each transistor for example corresponds to the length of each fin. In order to form the fins of the transistors, trenches are for example formed in one direction between the fins to delimit the width W_T of each transistor fin, and further trenches are for example formed in the perpendicular direction to delimit the length of each transistor fin.

The isolation trenches **104**, **106** of FIG. **1**A or fins of FIG. **1**B are for example formed during first and second phases, each involving a separate photolithography operation, as will now be described with reference to FIGS. **2**A, **2**B, **3**A and **3**B.

FIG. **2**A represents, in plan view, an example of a mask, referred to as an RX mask, used during a first phase to form the horizontal isolation trenches **106** of the SOI structure of FIG. **1**A or to delimit the widths W_T of the fins of FIG. **1**B, according to an example embodiment, three trenches **106** being illustrated in FIG. **2**A. Diagonally striped rectangular zones running from left to right in FIG. **2**A represent the zones, labelled RX, on either side of the isolation trenches **106** in which the mask is present. The isolation trenches **106** for example have a width of between 30 and 300 nm.

FIG. **2**B represents, in plan view, an example of another mask, referred to as an RC mask, used during a second phase to form the vertical isolation trenches **104** of the SOI structure of FIG. **1**A or to delimit the lengths L_T of the fins of FIG. **1**B, according to an example embodiment, three trenches **104** being illustrated in FIG. **2**B. In this example, the RC mask is applied after the RX mask of FIG. **2**B has already been used to form the isolation trenches **106**. Blank zones, labelled RC, running from top to bottom in FIG. **2**A represent the zones in which the isolation trenches **104** are formed. The isolation trenches **104** for example have a width of between 30 and 300 nm.

FIGS. **3**A and **3**B show similar plan views to those of FIGS. **2**A and **2**B respectively, but corresponding to the case that the RC mask is applied during the first phase as shown in FIG. **3**A, and the RX mask is applied during the second phase as shown in FIG. **3**B.

Methods of applying stress to the semiconductor layer **112** of FIG. **1**A will now be described with reference to the cross-section views of FIGS. **4**A to **4**C, FIGS. **5**A to **5**C, and FIGS. **6**A to **6**D. Such methods are for example used to apply a uniaxial stress, but in some embodiments these methods could equally be used to apply a biaxial stress, if for example applied along both the transistor widths and lengths. Furthermore, in some embodiments, the semiconductor layer **112** may be pre-stressed to a certain level, and the methods described hereafter can be used to uniaxially enhance the stress, uniaxially relax the stress and/or uniaxially change the stress from a tensile stress to a compressive stress, or vice versa. Furthermore, it will be apparent to those skilled in the art how the teaching could equally be applied to the finFET embodiment of FIG. **1**B.

FIGS. **4**A to **4**C and **5**A to **5**C are cross-section views corresponding to cross-sections taken along the dashed line A-A' shown in FIG. **2**A, in the vertical direction and passing perpendicular to the mask zones RX. The cross-sections of FIGS. **4**A to **4**C and **5**A to **5**C also correspond to cross-sections taken along the dashed line A-A' shown in FIG. **3**A, in the horizontal direction and passing perpendicular to the mask zones RC. In other words, the horizontal and vertical trenches **106**, **104** being formed in first and second phases, these methods are for example applied during the first phase corresponding to FIGS. **2**A and **3**A. Alternatively, it will be apparent from the following description that these methods could additionally or alternatively be applied during the second phase corresponding to FIGS. **2**B and **3**B.

With reference to FIG. **4**A, it is assumed that the structure initially comprises the substrate **108**, insulator layer **110**, and semiconductor layer **112**, and that the following layers have also been formed over the SOI structure:

- a sacrificial oxide layer **402** overlying the semiconductor layer **112**, for example used during well implantation;
- a layer **404** of SiN, for example of between 40 and 60 nm in thickness, formed over layer **402**;
- a hard mask layer **406**, for example of between 40 and 60 nm, formed of TEOS or another suitable material, and formed over the layer **404**;
- a spin-on carbon (SOC) and/or silicon anti-reflective coating (SiARC) layer **408** formed over the hard mask layer **406**, and for example having a thickness of between 200 and 300 nm; and
- a photo resist layer **410** formed over layer **408**, and for example having a thickness of between 100 and 200 nm.

It will be apparent to those skilled in the art that one or more of the above layers could be omitted in some embodiments, such as any of the layers **402**, **404** and **406**.

As shown in FIG. **4**A, during a photolithography operation, the photo resist layer **410** is patterned, and trenches **412** are formed. The photo resist layer **410** is for example patterned by the RX or RC mask of FIG. **2**A or **3**A, the regions of hard mask **406** between the trenches **412** corresponding to the zones RX of FIG. **2**A, or the trenches themselves corresponding to the zones RC of FIG. **3**A. The trenches **412** are for example of shallower depth than the isolation trenches **104**, **106**, and for example extend to the sacrificial oxide layer **402**, above the semiconductor layer **112**, or at the surface of the semiconductor layer **112** in the case that there is no oxide layer **402**.

As shown in FIG. **4**B, the layers **408** and **410** are for example removed by an appropriate etching step, and an implantation **414** is performed via the trenches **412**, to implant atoms into regions **416** of the semiconductor layer **112**. For example, the implantation is of germanium, at an energy level of around 40 KeV, for example between 30 KeV and 50 KeV, and at a density of between 10^{14} and 5×10^{14} atoms/cm^3.

This implantation **414** for example renders amorphous the regions **416** of the semiconductor layer **112** below each trench **412**. For example, the regions **416** become amorphous SiGe regions in the case that the semiconductor layer **112** is of silicon or SiGe, and the implantation is of germanium.

Annealing is then performed to temporally decrease the viscosity of the insulator layer **110**, and also to cause a tensile stress to be exerted by the regions **416** into the portions of the semiconductor layer **112** on each side of these regions **416**.

The phenomenon of stress induced by amorphization and annealing is for example discussed in more detail in the publication entitled "Molecular Dynamic Simulation Study of Stress Memorization in Si Dislocations", Tzer-Min Shen et al., Research and Development, Taiwan Semiconductor Manufacturing Company (TSMC), the contents of which is hereby incorporated by reference to the extent allowable by the law.

For example, the insulator layer **110** is formed of silicon dioxide, and the decrease in the viscosity of the insulator layer **110** is achieved by annealing at between 950° C. and 1150° C., for 15 minutes or more. For example, the anneal is performed at between 950° C. and 1050° C. for a duration of between 30 and 60 minutes, or at between 1050° C. and 1150° C. for a duration of between 15 and 45 minutes. Alternatively, the insulator layer **110** could be formed of a material that is naturally of lower viscosity than silicon dioxide, for example of BPSG (boron phosphor silicon glass), and the anneal is performed at between 900° C. and 1100° C. for 5 minutes or more. For example, the anneal is performed at between 900° C. and 1000° C. for a duration of between 15 and 30 minutes, or at between 1000° C. and 1100° C. for a duration of between 5 and 20 minutes. By temporally decreasing the viscosity of the insulator layer **110**, the insulator layer **110** for example relaxes such that, when it cools again and the viscosity is increased, the stress in the semiconductor layer **112** is maintained not only by the regions **116**, but also by the underlying insulator layer **110**.

As shown in FIG. **4**C, the depth of the trenches **412** is extended by a further etching step to form trenches **412'** corresponding to the isolation trenches **104** or **106**. In doing so, all or most of the atoms implanted into the semiconductor layer **112** via the trenches **412** are removed, and some relaxation of the semiconductor layer **112** occurs. However, a certain level of stress is mechanically maintained in the semiconductor layer **112** by the insulator layer **110**.

For example, in the case that the channel to be formed in the resulting stressed semiconductor layer is an n-type channel, in order to exert a tensile stress on the channel region in the length L_T direction, the implantation is for example applied to the trenches **412** formed by the RC mask of FIG. **3**A.

Alternatively, in the case that the channel to be formed in the resulting stressed semiconductor layer is a p-type channel, in order to exert a tensile stress on the channel region in the width W_T direction, the implantation is for example applied to the trenches **412** formed by the RX mask of FIG. **2**A.

FIGS. **5**A to **5**C illustrate operations for applying a stress in the semiconductor layer **112** as an alternative to those of FIGS. **4**A to **4**C described above.

As shown in FIG. **5**A, the initial structure is for example substantially identical to that of FIG. **4**A, and will not be described again in detail. However, a difference is that, rather than the trenches **412** being formed, which extend to the sacrificial oxide layer **402**, deeper trenches **502** are formed in the same locations as the trenches **412**. The deeper trenches **502** for example extend to the upper surface of, or partially into, the insulator layer **110**.

As shown in FIG. **5**B, the layers **408** and **410** are for example removed by an appropriate etching step, and a layer **504** of a stress material is deposited, for example by CVP (chemical vapour deposition), filling the trenches **502**. The stress material is one that, when deposited in the trenches **502**, exerts a compressive or tensile stress, via the side walls of the trenches **502**, on the semiconductor layer **112**. For example, the stress material has a coefficient of thermal expansion (CTE) greater or lower than that of the material forming the semiconductor layer **112**, such that a stress is exerted when this material is heated.

After the layer **504** has been deposited, an annealing operation is for example performed to heat the stress material and the semiconductor layer **112**, causing the tensile or compressive stress to be generated, and also to temporally decrease the viscosity of the insulator layer **110**. For example, the insulator layer **110** is formed of silicon dioxide, and the decrease in the viscosity of the insulator layer **110** is achieved by annealing at between 950° C. and 1150° C., for 15 minutes or more. For example, the anneal is performed at between 950° C. and 1050° C. for a duration of between 30 and 60 minutes, or at between 1050° C. and 1150° C. for a duration of between 15 and 45 minutes. Alternatively, the insulator layer **110** could be formed of a material that is naturally of lower viscosity than silicon dioxide, for example of BPSG, and the anneal is performed at between 900° C. and 1100° C. for 5 minutes or more. For example, the anneal is performed at between 900° C. and 1000° C. for a duration of between 15 and 30 minutes, or at between 1000° C. and 1100° C. for a duration of between 5 and 20 minutes. By temporally decreasing the viscosity of the insulator layer **110**, the insulator layer **110** for example relaxes such that, when it cools again and the viscosity is increased, the stress in the semiconductor layer **112** is maintained not only by the regions **116**, but also by the underlying insulator layer **110**.

For example, in the case that the channel to be formed in the resulting stressed semiconductor layer **112** is an n-type channel, layer **112** is for example of silicon, and the deposited material for example has a lower CTE than silicon, in order to exert a tensile stress on the channel region in the length L_T direction when heated. In such a case, the trenches **502** for example correspond to those created by the RC mask of FIG. **3**A.

Alternatively, in the case that the channel to be formed in the resulting stressed semiconductor layer is a p-type channel, layer **112** is for example of SiGe, and the deposited material for example has a greater CTE than SiGe, in order to exert a compressive stress on the channel region in the length L_T direction when heated. In such a case, the trenches **502** for example correspond to those created by the RC mask of FIG. **3**A.

Examples of the stress material that can be used include Zirconium tungstate ZrW_2O_8 having a CTE of $-7.2\times10^{-6}K^{-1}$ lower than that of silicon, and Hafnium Oxide HfO_2 and titanium nitride TiN each having a CTE greater than that of silicon germanium.

As shown in FIG. **5**C, the depth of the trenches **502** is extended by a further etching step to form trenches **502'** corresponding to the isolation trenches **104** or **106**. In doing so, material deposited in the trenches **502** is substantially or entirely removed, and some relaxation of the semiconductor layer **112** occurs. However, a certain level of stress is maintained mechanically in the semiconductor layer **112** by the insulator layer **110**.

FIGS. **6**A to **6**D are cross-section views illustrating an example of further operations performed, for example, after the operation of FIG. **4**C or **5**C.

As shown in FIG. **6**A, the isolation trenches **104** or **106** are for example formed by lining the trenches **412'/502'** with a layer of oxide **602**, and then with a layer of SiN **604**. The trenches are then filled with a layer **606** of insulating material such as oxide to form the isolation trenches **106** or **104** during the first phase of FIG. **2**A or **3**A.

The formation, during the second phase of FIG. **2**B or **3**B, of the further trenches **104** or **106** not yet formed, may be achieved in a standard fashion, using a standard photolithography operation.

Alternatively, during the second phase, prior to forming the further isolation trenches, the semiconductor layer **112** may be stressed again, but in the orthogonal direction, with the same type of stress to the one introduced during the first phase, using the method of FIGS. **4**A to **4**C.

As a further alternative, during the second phase, prior to forming the further isolation trenches, the semiconductor layer **112** may be stressed again, but in the orthogonal direction, with the same or opposite type of stress to the one introduced during the first phase, using the method of FIGS. **5**A to **5**C, as will now be described with reference to FIGS. **6**B to **6**D.

FIGS. **6**B to **6**D are cross-section views corresponding to cross-sections taken along the dashed line B-B' shown in FIG. **2**B, in the horizontal direction and passing perpendicular to the mask zones RC. The cross-sections of FIGS. **6**B to **6**D also correspond to cross-sections taken along the dashed line B-B' shown in FIG. **3**B, in the vertical direction and passing perpendicular to the mask zones RX.

As shown in FIG. **6**B, a spin-on carbon (SOC) and/or silicon anti-reflective coating (SiARC) layer **608** is formed over the hard mask layer **406**, and for example has a thickness of between 200 and 300 nm. Furthermore, a photo resist layer **610** is formed over layer **608**, and for example has a thickness of between 100 and 200 nm.

During a photolithography operation, the photo resist **610** is patterned, and trenches **612** are formed. The photo resist is for example patterned as the masks shown in FIG. **2**B or **3**B, the trenches **612** corresponding to the zones RC of FIG. **2**B, or the regions of hard mask **406** between the trenches corresponding to the zones RX of FIG. **3**B. However, the trenches **612** for example have a shallower depth than the isolation trenches **104**, **106**, and for example extend down to the surface of, or partially into, the insulator layer **110**.

As shown in FIG. **6**C, the layers **608** and **610** are removed, for example by an appropriate etching, and a layer **614** of a stress material is deposited, for example by CVP (chemical vapour deposition), filling the trenches **612**. The stress material is for example selected having a CTE that, when heated, enhances the uniaxial stress in the semiconductor layer **112**. Therefore, if a tensile stress was applied to the semiconductor layer **112** during the first phase, during the second phase a compressive stress is for example applied, and vice versa.

As with the operation of FIG. **5**B, an annealing operation is for example performed to heat the stress material and the semiconductor layer **112**, causing the tensile or compressive stress to be generated, and also to temporally decrease the viscosity of the insulator layer **110**. For example, the insulator layer **110** is formed of silicon dioxide, and the decrease in the viscosity of the insulator layer **110** is achieved by annealing at between 950° C. and 1150° C., for 15 minutes or more. For example, the anneal is performed at between 950° C. and 1050° C. for a duration of between 30 and 60 minutes, or at between 1050° C. and 1150° C. for a duration of between 15 and 45 minutes. Alternatively, the insulator layer **110** could be formed of a material that is naturally of lower viscosity than silicon dioxide, for example of BPSG, and the anneal is performed at between 900° C. and 1100° C. for 5 minutes or more. For example, the anneal is performed at between 900° C. and 1000° C. for a duration of between 15 and 30 minutes, or at between 1000° C. and 1100° C. for a duration of between 5 and 20 minutes.

As shown in FIG. **6**D, an operation similar to that of FIG. **5**C is performed in which the depth of the trenches **612** is extended by a further etching step to form the isolation trenches **104** or **106**, the stress material being partially or entirely removed in the process.

FIG. **7** is a flow diagram illustrating operations in a method of forming a stressed semiconductor layer.

In an operation **702**, partial trenches in a first direction are formed in a surface of a semiconductor structure having a semiconductor layer in contact with an insulator layer. The trenches are partial in that they are for example shallower than the full depth isolation trenches that are to be formed. For example the partial trenches stop before the semiconductor layer **112** in the example of FIG. **4**A, or extend to the surface of or into the insulator layer **110** in the example of FIG. **5**A.

In operation **704**, a stress is introduced into the semiconductor layer via the partial trenches, for example by introducing a material, such as atoms implanted into the semiconductor layer, and annealing, as described above with reference to FIG. **4**B, or by depositing a stress material in the trenches at the level of the semiconductor layer, and annealing, as described above with reference to FIGS. **5**B and **6**C. Furthermore, the viscosity of the insulator layer is temporally decreased by the annealing, while maintaining the stress in the semiconductor layer.

In operation **706**, the depth of the partial trenches is extended to form isolation trenches in the first direction delimiting a dimension, such as the transistor width W_T or length L_T, of a transistor to be formed in the semiconductor structure.

FIGS. **8**A to **8**D are cross-section views illustrating operations in a method of forming a semiconductor layer with uniaxial stress according to a further example embodiment of the present disclosure. Such a method is for example used to transform a semiconductor layer having biaxial stress into one having uniaxial stress, and/or to conserve or enhance uniaxial stress already present in a semiconductor layer. For example, the method of FIGS. **8**A to **8**D could be applied to the structure of FIG. **4**C or **5**C described above, or the steps of FIGS. **6**A to **6**D could be adapted to incorporate the method of FIGS. **8**A to **8**D. Alternatively, the method of FIGS. **8**A to **8**D may be performed independently of any previously described method. It will also be apparent to those skilled in the art how the method of FIGS. **8**A to **8**D could be applied to the FinFET structure of FIG. **1**B.

The cross-section views of FIGS. **8**A and **8**B for example correspond to cross-sections taken along the dashed line A-A' of FIG. **2**A or **3**A.

As shown in FIG. **8**A, the initial structure is for example the same as that of FIGS. **4**C and **5**C, and the layers have been labelled with like reference numbers and will not be described again in detail. The trenches are however labelled **802** in FIG. **8**A, and could correspond to the trenches **412**' or **502**' described above. Indeed, these trenches **802** correspond to isolation trenches, not yet filled with an insulating material, that delimit one of the dimensions of the transistor to be formed, for example the transistor length L_T or width W_T, and for example extend through the SOI structure at least down to the insulator layer **110**, and for example into the substrate **108**.

FIG. **8**B illustrates an operation in which the trenches **802** are lined with the oxide and SiN layers **602** and **604** as described above, and the layer **606** of insulating material, such as oxide, is deposited filling the trenches **802**.

As represented by double-headed arrows in FIGS. **8**A and **8**B, before and/or after the filling of the trenches **802** with oxide, an annealing operation is performed to uniaxially relax the stressed semiconductor layer **112** by temporally decreasing the viscosity of the insulator layer **110**. For example, the insulator layer **110** is formed of silicon dioxide, and the decrease in the viscosity of the insulator layer **110** is achieved by annealing at between 950° C. and 1150° C., for 15 minutes or more. For example, the anneal is performed at between 950° C. and 1050° C. for a duration of between 30 and 60 minutes, or at between 1050° C. and 1150° C. for a duration of between 15 and 45 minutes. Alternatively, the insulator layer **110** could be formed of a material that is naturally of lower viscosity than silicon dioxide, for example of BPSG, and the anneal is performed at between 900° C. and 1100° C. for 5 minutes or more. For example, the anneal is performed at between 900° C. and 1000° C. for a duration of between 15 and 30 minutes, or at between 1000° C. and 1100° C. for a duration of between 5 and 20 minutes.

With reference to FIGS. **2**A and **3**A, it will be noted that the relaxation resulting from this annealing operation is substantially uniaxial, because only trenches **104** or **106** have been formed, and thus the semiconductor layer forms strips that maintain stress along their length. Indeed, in the case of FIG.

2A, the trenches corresponding to the isolation trenches **106** have been formed, and thus there will be relaxation in the perpendicular direction, as shown by double headed arrows in this figure. In the case of FIG. **3**A, the trenches corresponding to the isolation trenches **104** have been formed, and thus relaxation will occur in the perpendicular direction shown by double headed arrows in this figure.

FIG. **8**C shows an operation, and illustrates the cross-section B-B' of FIG. **2**B or **3**B. As illustrated, trenches **804** are formed, which for example correspond to trenches **612** of FIG. **6**D, or result from a standard photolithography operation.

As shown in FIG. **8**D, the trenches **804** are lined with the oxide and SiN layers **616** and **618** as described above, and the layer **620** of insulating material, such as oxide, is deposited filling the trenches **804**. An annealing of the isolation trenches is then performed, for example at the same temperature and duration as the annealing operation described above in relation to FIG. **8**B. While annealing the isolation trenches may lead to a further relaxation of the stressed semiconductor layer **112**, such a relaxation will be biaxial, and thus the uniaxial nature of the stress will be at least partially maintained. Furthermore, annealing of the isolation trenches may be performed at a reduced temperature, and/or for a reduced duration, in order to limit the decrease in the viscosity of the insulator layer **110**, and thus enhance conservation of the uniaxial stress.

FIG. **9** is a flow diagram illustrating operations in a method of forming a semiconductor layer having uniaxial stress.

In operation **902**, at least two first trenches are formed in the surface of the semiconductor structure in a first direction delimiting a first dimension, such as the transistor width W_T or length L_T, of at least one first transistor to be formed in the semiconductor structure. As mentioned above in relation to FIGS. **8**A to **8**D, the semiconductor layer is for example pre-stressed uniaxially or biaxially.

The formation of the first trenches may or may not include the filling of the trenches with a layer of insulating material.

In operation **904**, a first anneal is performed to decrease the viscosity of the insulator layer of the semiconductor structure. For example, the first anneal is performed at a temperature of between 1000° C. and 1150° C., and for a duration of at least 30 minutes.

In operation **906**, at least two second trenches are formed in the semiconductor structure in a second direction delimiting a second dimension of the at least one transistor. In the case that the first dimension is the transistor length L_T, the second dimension is for example the transistor width W_T, and vice versa.

The second trenches are then for example filled with an insulating material, such as a layer of oxide. In the case that the first trenches were not also filled with insulating material during the operation **902**, these trenches are also for example filled at the same time as the second trenches.

Optionally, the method further comprises an operation **908** in which a second anneal is performed, to heat the isolation trenches. The second anneal is for example performed at a temperature of between 900 and 1000° C., and for a duration of between 15 and 30 minutes.

For example, in the case that the channel to be formed in the resulting stressed semiconductor layer is an n-type channel, initially the semiconductor layer **112** for example has biaxial tensile stress, and in order to relax the channel region in the width W_T direction, the first trenches for example correspond to those formed using the RX mask of FIG. **2**A.

Alternatively, in the case that the channel to be formed in the resulting stressed semiconductor layer is a p-type channel, initially the semiconductor layer **112** for example has biaxial compressive stress, and in order to relax the channel region in the width W_T direction, again the first trenches for example correspond to those formed using the RX mask of FIG. **2**A.

FIGS. **10**A to **10**C are cross-section views illustrating operations in a method of forming a semiconductor layer with uniaxial stress according to an example embodiment of the present disclosure. In particular, this method is for example used to transform a semiconductor layer having biaxial stress into one having uniaxial stress, and/or to conserve or enhance uniaxial stress already present in a semiconductor layer.

For example, the method of FIGS. **10**A to **10**C could be applied to the structure of FIG. **4**C or **5**C described above, or the steps of FIGS. **6**A to **6**D or FIGS. **8**A to **8**D could be adapted to incorporate such a method. Alternatively, the method of FIGS. **10**A to **10**C may be performed independently of any previously described method. Furthermore, rather than being applied to isolation trenches of an SOI structure, the method of FIGS. **10**A to **10**C could equally be applied to isolation trenches of a bulk silicon structure, or to the trenches between the fins in the FinFET structure of FIG. **1**B.

The cross-sections of FIGS. **10**A to **10**C for example corresponds to the cross-section indicated by the dashed line A-A' in FIG. **2**A or FIG. **3**A, or to those indicated by the dashed line B-B' in FIG. **2**B or FIG. **3**B.

As shown in FIG. **10**A, the initial structure is for example the same as that of FIGS. **4**C and **5**C, and the layers have been labelled with like reference numbers and will not be described again in detail. The trenches are however labelled **1002** in FIG. **10**A, and for example correspond to the trenches **412**' or **502**' of FIGS. **4**C and **5**C, the trenches **612** of FIG. **6**D, the trenches **802** of FIG. **8**B or the trenches **804** of FIG. **8**D. These trenches **1002** correspond to isolation trenches, filled with an insulating material such as oxide, that delimit one of the dimensions of the transistor to be formed, for example the transistor length L_T or width W_T, and for example extend through the SOI structure at least into the insulator layer **110**, and for example into the substrate **108**.

A dashed-dotted line **1003** in FIG. **10**A represents a level down to which the device is for example to be planarized. Such a planarization for example leads to a certain relaxation of the stressed semiconductor layer **112**, whether the device has an SOI or bulk structure.

As shown in FIG. **10**B, a SOC (spin on carbon) or and/or silicon anti-reflective coating (SiARC) layer **1004** is formed over the semiconductor structure, and a photo resist layer **1006** is deposited over layer **1004**. A photolithography operation is then used to form trenches **1008**, each of which is for example aligned over a corresponding one of the trenches **1002**. The trenches **1008** for example each extend to the surface of the layer **606** of insulating material. The trenches are for example formed using a mask similar to the RX or RC masks of FIGS. **2**A, **2**B, **3**A and **3**B.

An implantation is then for example performed, into each of the trenches **1002**, via the corresponding trenches **1008**. For example, the implantation is of a material altering the viscosity of the insulating material filling each of the trenches **1002**. In one example, the material is boron or phosphorus, implanted at a concentration of between 10^{12} and 10^{14} atoms/cm^3, and at an energy of between 70 and 150 keV for boron, or at an energy of between 200 and 300 keV for phosphorus, depending on the layers present above the trenches.

As shown in FIG. **10**C, the device is planarized, for example by a CMP (chemical-mechanical polishing) operation, down to the level of the dashed-dotted line **1003**. As shown by double-headed arrows in FIG. **10**C, the removal of one or more of the layers overlying the semiconductor layer **112** causes a relaxation, which is enhanced in the direction of the cross-section A-A' due to the decreased viscosity of the insulating material filling the trenches **1002**.

FIG. **11** is a flow diagram illustrating operations in a method of forming a semiconductor layer having uniaxial stress according to an example embodiment.

In a first operation **1102**, one or more first isolation trenches are formed in a first direction for delimiting a first dimension, such as the transistor width W_T or length L_T, of one or more transistors to be formed.

In operation **1104**, one or more second isolation trenches are formed in a second direction for delimiting a second dimension, such as the transistor length L_T, or width W_T of the one or more transistors.

In operation **1106**, the viscosity of the insulating material filling the first trenches is decreased by selectively implanting atoms of a material into the first isolation trenches and not into the second isolation trenches. In some embodiments, this implantation operation may be performed before the second isolation trenches are formed in operation **1104**.

In operation **1108**, an annealing operation is optionally performed, corresponding for example to an annealing of the isolation trenches after the implantation operation **1106**.

In operation **1110**, one or more layers, for example including a hard mask layer, overlying the semiconductor layer, are removed. In some embodiments, these one or more layers include a layer formed directly over the semiconductor layer.

For example, in the case that the channel to be formed in the resulting stressed semiconductor layer is an n-type channel, in order to maintain a tensile stress in the channel region in the transistor length L_T direction, the first trenches for example correspond to those formed using the RC mask of FIG. **3**A.

Alternatively, in the case that the channel to be formed in the resulting stressed semiconductor layer is a p-type channel, in order to maintain a compressive stress in the channel region in the length L_T direction, the first trenches for example correspond to those formed using the RX mask of FIG. **2**A.

An advantage of the various embodiments described herein is that uniaxial stress may be introduced or enhanced in a semiconductor layer in a simple and low cost manner. Such a uniaxial stress has the advantage of providing an improved mobility of charge carriers in the channel region of a transistor when compared to a semiconductor layer having a similar level of biaxial stress. In particular, it has been found by the present inventors that enhancing uniaxial stress, for example by introducing stress in one direction or by relaxing a biaxially stressed semiconductor layer in one direction, can lead to a performance gain. For example, in a p-type channel, mobility of charge carriers can be enhanced by the presence of compressive stress in the transistor length direction, and a relaxation or tensile stress in the transistor width direction. In an n-type channel, mobility of charge carriers can be enhanced by the presence of tensile stress in the transistor length direction, and a relaxation or compressive stress in the transistor width direction.

Having thus described at least one illustrative embodiment, various alterations, modifications and improvements will readily occur to those skilled in the art.

For example, while specific examples of layers and material that may be used during the various photolithography steps have been described, it will be apparent to those skilled in the art that there are a broad range of equivalent techniques that could be used, employing layers of different materials.

Furthermore, it will be apparent to those skilled in the art that the various features described in relation to the various embodiments described herein may be combined, in alternative embodiments, in any combination.

The various embodiments described above can be combined to provide further embodiments. These and other changes can be made to the embodiments in light of the above-detailed description. In general, in the following claims, the terms used should not be construed to limit the claims to the specific embodiments disclosed in the specification and the claims, but should be construed to include all possible embodiments along with the full scope of equivalents to which such claims are entitled. Accordingly, the claims are not limited by the disclosure.

The invention claimed is:

1. A method of forming a stressed semiconductor layer, the method comprising:

forming, in a surface of a semiconductor structure having a semiconductor layer in contact with an insulator layer having a viscosity, at least two first trenches having a first depth in a first direction;

introducing, through said at least two first trenches, a stress in said semiconductor layer and temporarily decreasing, by annealing, the viscosity of said insulator layer; and

forming in said first direction first isolation trenches delimiting a first dimension of at least one transistor to be formed in said semiconductor structure by extending said at least two first trenches from a first depth to a second depth.

2. The method of claim **1**, wherein introducing the stress in said semiconductor layer comprises introducing a first material through said at least two first trenches and annealing the first material, and wherein extending said at least two first trenches from the first depth to a second depth comprises at least partially removing said first material.

3. The method of claim **2**, wherein introducing said first material comprises:

implanting atoms of said first material into a region of said semiconductor layer underlying each of said at least two first trenches; or

depositing said first material to at least partially fill each of said at least two first trenches, and wherein annealing the first material comprises heating said first material.

4. The method of claim **2**, wherein introducing said first material comprises implanting atoms of said first material into regions of said semiconductor layer, wherein said first depth of said at least two first trenches does not extend into said semiconductor layer.

5. The method of claim **4**, wherein said first material is germanium.

6. The method of claim **2**, wherein introducing said first material comprises depositing said first material to at least partially fill each of said at least two first trenches, and said first depth of said at least two first trenches extends through said semiconductor layer and at least partially into said insulator layer.

7. The method of claim **6**, wherein introducing said first material comprises depositing a metal to at least partially fill said at least two first trenches.

8. The method of claim **6**, wherein said first material has a first coefficient of thermal expansion and said semiconductor layer has a second coefficient of thermal expansion that is different from the first coefficient of thermal expansion.

9. The method of claim **6**, wherein said first material has a first coefficient of thermal expansion and the semiconductor layer has a second coefficient of thermal expansion that is different from the first coefficient of thermal expansion, the method further comprising, prior to temporarily decreasing the viscosity of said insulator layer:

forming, in said surface of said semiconductor structure, at least two second trenches in a second direction;

depositing a second material to at least partially fill each of said at least two second trenches, wherein said second material has a third coefficient of thermal expansion that is different from the first and second coefficients of thermal expansion; and

forming second isolation trenches in said second direction delimiting a second dimension of said at least one transistor by extending said at least two second trenches from a first depth to a second depth.

10. The method of claim **1**, further comprising forming at least two second isolation trenches in a second direction delimiting a second dimension of said at least one transistor.

11. The method of claim **10**, wherein forming said at least two second isolation trenches is performed after temporarily decreasing the viscosity of the insulator layer.

12. The method of claim **1**, wherein said annealing comprises annealing between 950° C. and 1150° C. for at least 20 minutes.

13. The method of claim **1**, wherein said semiconductor structure is an SOI (semiconductor on insulator) structure.

14. The method of claim **1**, wherein said semiconductor layer comprises a plurality of semiconductor fins.

15. A method comprising:

in a semiconductor structure that includes a semiconductor layer located on an insulator layer having a viscosity, forming a plurality of trenches having a first depth in a first direction;

introducing a material in the plurality of trenches;

stressing the semiconductor layer and temporarily decreasing the viscosity of the insulator layer by annealing the semiconductor structure; and

after annealing, forming first isolation trenches in the first direction for delimiting in a first dimension a transistor to be formed in the semiconductor structure by extending the two trenches from a first depth to a second depth, the second depth being deeper than the first depth.

16. The method of claim **15**, wherein introducing the material comprises depositing the material to at least partially fill the trenches.

17. The method of claim **15**, wherein the material has a first coefficient of thermal expansion and the semiconductor layer has a second coefficient of thermal expansion that is different from the first coefficient of thermal expansion.

18. The method of claim **15**, wherein the material is germanium.

19. The method of claim **15**, wherein the second depth extends into a semiconductor substrate of the structure that is located below the semiconductor layer and the insulator layer.

20. The method of claim **15**, wherein the first depth of the plurality of trenches does not extend into the semiconductor layer located on the insulator layer.

21. The method of claim **20**, wherein introducing the material comprises implanting atoms of the material into a region of the semiconductor layer that underlies the plurality of trenches.

22. The method of claim **15**, further comprising forming the transistor in the semiconductor structure.

23. A method comprising:

in a semiconductor structure that includes a semiconductor layer located on an insulator layer having a viscosity, forming a plurality of trenches having a first depth in a first direction;

introducing a material in the plurality of trenches;

stressing the semiconductor layer and temporarily decreasing the viscosity of the insulator layer by annealing the semiconductor structure;

after annealing the semiconductor structure, forming first isolation trenches in the first direction for delimiting in a first dimension a transistor to be formed in the semiconductor structure by extending the two trenches from a first depth to a second depth, the second depth being deeper than the first depth; and

forming the transistor in the semiconductor structure.

24. The method of claim **23**, wherein introducing the material comprises depositing the material to at least partially fill the trenches.

25. The method of claim **23**, wherein the material has a first coefficient of thermal expansion and the semiconductor layer has a second coefficient of thermal expansion that is different from the first coefficient of thermal expansion.

26. The method of claim **23**, wherein the material is germanium.

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